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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,458	09/18/2001	Choong-Keun Kwak	8045-22 (PX1255-US/SSM)	9405

22150 7590 08/23/2005

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,458	KWAK ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6,8-11 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 6, 8-11, and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Jun 22, 2005 was reviewed and considered with the following results:

The amended change to the paragraph on page 8 overcame its objection, which has now been withdrawn.

The cancellation of claim 5 rendered it objection and rejection moot.

Amended claim 1 overcame the objections to claims 1, 3, and 5. Those objections have also been withdrawn.

Amended claim 17 overcame the rejections of claims 17-18 under 35 U.S.C. 112. Although these rejections have been withdrawn, some amended changes created new rejections that are described later under the appropriate section.

Amended claim 1 overcame the rejections of claims 1, and 3 under 35 U.S.C. 102(b) with respect to Oh, and these rejections have been withdrawn. Oh does not show/disclose a voltage supply circuit (with a PMOS transistor and a plurality of NMOS transistors) for supplying the enable voltage to the gates of the plurality of MOS transistors as now recited within claim 1, upon which claim 3 depends.

Amended claims 6 and 16 also overcame their corresponding prior art rejections as described in the previous Office Action. Although those rejections (i.e. 6, 8-11, and 13-15 under 35 U.S.C. 103(a) with respect to Viehmann; and claims 6, 8-11, and 13-16 under 35 U.S.C. 103(a) with respect to Taguchi) have now all been withdrawn because neither Viehmann nor

Taguchi shows/discloses the voltage supply circuit as now recited within independent claims 6 and 16, the claims are now rejected with respect to another prior art reference.

After reconsidering the claim limitations, it was determined that a voltage supply circuit with a PMOS transistor and a plurality of NMOS transistors is known to one of ordinary skill in the art, and it would be obvious to use it to provide the voltage to the gate of the transistor providing the active resistance. Therefore, new prior art rejections are described later under the appropriate section.

Therefore, this Office Action is **NON-FINAL**.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Since claim 7 was cancelled, claims 8-11 now depend on a non-existent active claim.

Claim 16 recites the limitations "the enable voltage" and "the plurality of MOS transistors" in lines 19-20 with insufficient antecedent basis for these limitations in the claim.

Claim 18 recites the limitation ""the control signal" in line 4. There is insufficient antecedent basis for this limitation in the claim. For example, how does this signal relate to "the enable voltage" supplied by the voltage supply circuit of claim 16?

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 6, 8-11, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viehmann's PCT WO 01/61430 A1, (published in German on Aug 23, 2001), a reference cited in the previous Office Action, in view of Kokubo et al. (Kokubo), a newly cited reference. [Note: Viehmann's U.S. Patent 6,586,919 B2 (filed Aug 15, 2002), is considered an acceptable English translation of the PCT reference used in the above rejections.] Fig. 1 of Viehmann shows one type of reference voltage generating circuit comprising active resistance part 22 having single MOS transistor 22, wherein the circuit is connected between external voltage U_{DD} and a ground voltage (not labeled). The gate electrode of MOS transistor 22 receives enable voltage U_E, which is understood to have a higher potential than the drain to source voltage of MOS transistor 22, thus allowing MOS transistor 22 to operate in a linear current-voltage region

(e.g. see page 5, lines 5-15 with respect to "Drain-Source-Spannung...60 mV"; "Eingangsspannung zwischen 2 und 5 Volt"; "Gate-Source-Spannung... Eingangsspannung"; "als "linearer Bereich" oder "aktiver Bereich"."). Therefore, it is understood the active resistance device operates in the linear region. Fig. 1 also shows current mirror circuit 20 having first/second current paths 30,24,22/32,26 formed between first power source terminal U_{DD} and a second power source terminal (e.g. ground), wherein the current mirror circuit is operated in response to a voltage level of the second current path (e.g. via the voltage level between 32 and 26 being applied to the gate of 30); although a reference voltage output node is not specifically shown on the second current path (between 32 and 26) for providing a reference voltage (e.g. see page 9, line 22 "Transistor 26 abfallende Spannungsabfall U_{26}"), it would be obvious to one of ordinary skill in the art that the common node between 32 and 26 could be used to provide a reference voltage output node. However, the reference does not show or disclose a voltage supply circuit, with a PMOS transistor and a plurality of NMOS transistors, for supplying enable voltage U_E. Fig. 1 of Kokubo shows voltage supply circuit 4 providing voltage V(8) to the gate of NMOS transistor 64. Circuit 4 comprises PMOS transistor 2, and NMOS transistors 1a-1d. Voltage V(8) is disclosed as being constant and independent of the power supply voltage (e.g. see column 6, lines 40, and 52-60). Therefore, it would have been obvious to one of ordinary skill in the art to use voltage supply circuit 4 of Kokubo to supply voltage V(8) as enable voltage U_E. supplied to the gate of MOS transistor 22, thus rendering claim 6 obvious. Kokubo's circuit is one known means for providing a stable reference voltage to an NMOS transistor. Since active resistance device 22 is a single MOS transistor, and enable voltage U_E (e.g. 2 to 5 volts; or 3 * Vthn as disclosed by Kokubo on column 6, line 58) would be higher than the drain to source

voltage of a MOS transistor, claims 8-9 are rendered obvious. Also, it would have been obvious to one of ordinary skill in the art to replace active resistance device 22 with a plurality of series coupled N-channel MOS transistors that all receive the enable/control gate voltage, rendering claim 10 obvious, and also claim 1. The single MOS transistor 22, shown in the figure, could be replaced by a functionally equivalent plurality of series coupled NMOS transistors to be used as the active resistance device depending on the overall size requirements of the elements (or circuit), and/or voltage levels required. For example, a plurality of series connected small MOS transistors can provide the same resistance (and voltage drop) as a single, large MOS transistor. To ensure the active resistance device's transistors operate in the linear region, the enable voltage applied to the gates would be higher than the drain to source voltages of the NMOS transistors, and claim 11 is also rendered obvious. Deeming U_{DD} as an externally applied voltage applied to the first power source terminal, and ground is connected to the second power source terminal (i.e. the sources of 22 and 26), claims 13 and 3 are rendered obvious. Current control unit 24,26, with MOS transistors 24/26 formed on the first/second current paths, respectively, controls the current flowing in those paths, rendering obvious claim 14. Since current mirror circuit 20 includes a pair of PMOS transistors 30/32 formed on the first/second current paths, respectively, claim 15 is also rendered obvious.

Claims 1, 3, 6, 8-11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi, a reference cited in the previous Office Action, in view of Kokubo (the reference identified in the rejections described above). Fig. 12 of Taguchi shows a reference voltage generating circuit that directly corresponds to the applicants' own Prior Art Fig. 2. Taguchi's reference comprises current mirror circuit 50,51 having first/second current paths 50,41,42/51,39

formed between first power source terminal 37 (receiving voltage VCC) and a second power source terminal (ground), wherein the current mirror circuit is operated in response to a voltage level (via the interconnections of the transistors) of the second current path; reference voltage output node 43, on the second current path, provides reference voltage Vref; and resistance device 42 is formed on the first current path. Although resistance device 42 is a passive device instead of an active resistance device, Taguchi discloses it as a load element (e.g. see column 7, lines 46-47), wherein Taguchi also discloses load elements can be a resistor or an insulated-gate field-effect transistor (e.g. see column 6, lines 20-23; and column 7, lines 19-23). Therefore, it would have been obvious to one of ordinary skill in the art to replace resistance device 42 with a FET (one known type of active resistance device) operated in a linear region. However, the reference does not show or disclose that even if 42 is a FET, that its gate receives a voltage from a voltage supply circuit comprising a PMOS transistor and a plurality of NMOS transistors. Therefore, for the same reasoning as applied to the Viehmann/Kokubo rejections described above, it would have been obvious to one of ordinary skill in the art to use Kokubo's voltage supply circuit 4, thus rendering claim 6 obvious. When operated in the linear (e.g. triode, resistive, nonsaturation, or ohmic) region, the active resistance FET device will function as a resistor with a resistance that varies with the FET's control gate voltage being higher than the drain to source voltage. The FET would use less area than a resistor; help reduce power consumption; and allow the resistance to be changed (e.g. by adjustment of the gate voltage) to meet the desired requirement(s) of the overall circuit's use. Kokubo's circuit would ensure the voltage applied to the gate of the active resistance device/FET will remain constant, thus maintaining the resistance of the device constant. It would have been obvious to one of ordinary

skill in the art that the active resistance FET device could be a single N-channel MOS transistor, or a plurality of series coupled N-channel MOS transistors that all receive the enable/control gate voltage, rendering claims 8, 10, and 1 obvious. The single MOS transistor, or a functionally equivalent plurality of series coupled MOS transistors, can be used as the active resistance device depending on the overall size requirements of the elements (or circuit), and/or voltage levels required. For example, a plurality of series connected small MOS transistors can provide the same resistance (and voltage drop) as a single, large MOS transistor. To ensure the active resistance device's transistor(s) operates in the linear region, the enable voltage applied to the gate(s) would be higher than the drain to source voltage(s) of the N-channel MOS transistor(s), and claims 9 and 11 are rendered obvious. For example, by using Kokubo's voltage supply circuit, the enable voltage would be 3*Vthn (e.g. see column 6, line 58). Since first power source terminal 37 receives externally applied voltage VCC, and the second power source terminal is connected to a ground voltage (not labeled but understood), claims 13 and 3 are also rendered obvious. The Fig. 12 circuit also comprises current control unit 41,39 for controlling current flowing in the first/second current paths by employing MOS transistors 41,39 formed on the first/second current paths, respectively. These transistors render claim 14 obvious. Since current mirror circuit 50,51 includes a pair of PMOS transistors 50/51 formed on the first/second current paths respectively, claim 15 is also rendered obvious. Interpreting Fig. 12 in a slightly different manner, it shows a reference voltage generating circuit comprising current mirror circuit 50,51 with first/second MOS transistors 50/51, wherein their sources receive externally applied voltage VCC, the gate of first MOS transistor 50 is connected to its drain, as well as to the gate of second MOS transistor 51; current control circuit 41,39 with third/fourth MOS

transistors 41/39, wherein the drains of first/third MOS transistors 50/41 are connected together, the drain of fourth MOS transistor 39 is connected to the gate of third MOS transistor 41 and to the drain of second MOS transistor 51, and a source of fourth MOS transistor 39 is connected to ground. The node between the drains of the second/fourth MOS transistors 51/39 provides reference voltage Vref. However, the reference shows passive resistance circuit 42 coupled between the source of third MOS transistor 41/gate of fourth MOS transistor 39 and ground. As previously described above, Taguchi discloses the resistance circuit (e.g. load or resistor) can be replaced with a MOS transistor. Therefore, it would have been obvious to one of ordinary skill in the art to replace resistance circuit 42 with an active resistance circuit, such as an NMOS transistor. This would be the fifth MOS transistor within the reference voltage circuit, and would have its drain coupled to the source of third MOS transistor 41 and to the gate of fourth MOS transistor 39; its source connected to ground; and to ensure the fifth MOS transistor operates in the linear region to provide the proper resistance, its gate could receive control voltage V(8), which is higher than the voltage between the transistor's drain and source, from Taguchi's voltage supply circuit. Therefore, claim 16 is rendered obvious.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 17-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensured the gate of the PMOS transistor

(within the voltage supply circuit) is connected to the drain of the first MOS transistor as recited within claim 17, upon which claim 18 depends.

Claims 2, 4-5, 7, and 12 have been cancelled.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

19 August 2005

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